

# PATENT COOPERATION TREATY

14 pages

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From the INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

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PCT

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## NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Rule 71.1)

FAX: +44 1252 383031

Date of mailing

(day/month/year)

14.06.2004

Applicant's or agent's file reference

XA1623

### IMPORTANT NOTIFICATION

International application No.

PCT/GB 02/05734

International filing date (day/month/year)

17.12.2002

Priority date (day/month/year)

02.01.2002

Applicant

BAE SYSTEMS PLC

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

#### 4. REMINDER

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices) (Article 39(1)) (see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

The applicant's attention is drawn to Article 33(5), which provides that the criteria of novelty, inventive step and industrial applicability described in Article 33(2) to (4) merely serve the purposes of international preliminary examination and that "any Contracting State may apply additional or different criteria for the purposes of deciding whether, in that State, the claimed inventions is patentable or not" (see also Article 27(5)). Such additional criteria may relate, for example, to exemptions from patentability, requirements for enabling disclosure, clarity and support for the claims.

Name and mailing address of the international preliminary examining authority:



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# PATENT COOPERATION TREATY

# PCT

## INTERNATIONAL PRELIMINARY EXAMINATION REPORT (PCT Article 36 and Rule 70)

Applicant's or agent's file reference <b>XA1623</b>	<b>FOR FURTHER ACTION</b> See Notification of Transmittal of International Preliminary Examination Report (Form PCT/PEA/416)	
International application No. <b>PCT/GB 02/05734</b>	International filing date (day/month/year) <b>17.12.2002</b>	Priority date (day/month/year) <b>02.01.2002</b>
International Patent Classification (IPC) or both national classification and IPC <b>H02M7/48</b>		
Applicant <b>BAE SYSTEMS PLC</b>		

1.	This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.
2.	<p>This REPORT consists of a total of 10 sheets, including this cover sheet.</p> <p><input checked="" type="checkbox"/> This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).</p> <p>These annexes consist of a total of 6 sheets.</p>
3.	<p>This report contains indications relating to the following items:</p> <ul style="list-style-type: none"> <li>I <input checked="" type="checkbox"/> Basis of the opinion</li> <li>II <input type="checkbox"/> Priority</li> <li>III <input checked="" type="checkbox"/> Non-establishment of opinion with regard to novelty, inventive step and industrial applicability</li> <li>IV <input type="checkbox"/> Lack of unity of invention</li> <li>V <input checked="" type="checkbox"/> Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement</li> <li>VI <input type="checkbox"/> Certain documents cited</li> <li>VII <input type="checkbox"/> Certain defects in the international application</li> <li>VIII <input type="checkbox"/> Certain observations on the international application</li> </ul>

Date of submission of the demand  <b>07.06.2003</b>	Date of completion of this report  <b>14.06.2004</b>
Name and mailing address of the international preliminary examining authority:  European Patent Office, D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized Officer  <b>Zettler, K-R</b>  Telephone No. +49 89 2399-7554 

**INTERNATIONAL PRELIMINARY  
EXAMINATION REPORT**

International application No. PCT/GB 02/05734

**I. Basis of the report**

1. With regard to the **elements** of the international application (*Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17)*):

**Description, Pages**

1-27 as originally filed

**Claims, Numbers**

1-31 filed with telefax on 02.06.2004

**Drawings, Sheets**

1/6-6/6 as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language: , which is:

- ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).  
☐ the language of publication of the international application (under Rule 48.3(b)).  
☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in written form.  
☐ filed together with the international application in computer readable form.  
☐ furnished subsequently to this Authority in written form.  
☐ furnished subsequently to this Authority in computer readable form.  
☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.  
☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:  
☐ the claims, Nos.:  
☐ the drawings, sheets:

**INTERNATIONAL PRELIMINARY  
EXAMINATION REPORT**

International application No. PCT/GB 02/05734

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)).

*(Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)*

6. Additional observations, if necessary:

**III. Non-establishment of opinion with regard to novelty, inventive step and industrial applicability**

1. The questions whether the claimed invention appears to be novel, to involve an inventive step (to be non-obvious), or to be industrially applicable have not been examined in respect of:

☐ the entire international application,

☒ claims Nos. 5,6,7,9-11,13,15-31

because:

☐ the said international application, or the said claims Nos. relate to the following subject matter which does not require an international preliminary examination (specify):

☐ the description, claims or drawings (*indicate particular elements below*) or said claims Nos. are so unclear that no meaningful opinion could be formed (*specify*):

☐ the claims, or said claims Nos. are so inadequately supported by the description that no meaningful opinion could be formed.

☒ no international search report has been established for the said claims Nos. 5,6,7,9-11,13,15-31

2. A meaningful international preliminary examination cannot be carried out due to the failure of the nucleotide and/or amino acid sequence listing to comply with the standard provided for in Annex C of the Administrative Instructions:

☐ the written form has not been furnished or does not comply with the Standard.

☐ the computer readable form has not been furnished or does not comply with the Standard.

**V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Yes: Claims	1-4,8,12,14
	No: Claims	
Inventive step (IS)	Yes: Claims	1-4,8,12,14
	No: Claims	
Industrial applicability (IA)	Yes: Claims	1-4,8,12,14
	No: Claims	

2. Citations and explanations

**see separate sheet**

**Re Item I**

**Basis of the report**

The amended claims 1-31 sent by fax on 2 June 2004 replace the claims 1-32 as originally filed. New claim 1 is based on the originally filed claims 1 and 2. The originally filed claims 3 to 32 are renumbered to the new claims 2 to 31, with the claim references adapted accordingly.

**Re Item III**

**Non-establishment of opinion with regard to novelty, inventive step and industrial applicability**

No opinion with regard to novelty, inventive step and industrial applicability is established for the claims 5, 6, 7, 9-11, 13, 15-31, because in the international search phase

- claims 15 and 29-31 have not been searched due to lack of clarity.
- lack of unity was identified. Since no required additional search fees were timely paid by the applicant, the International Search Report, and with it the International Preliminary Examination, is restricted to the invention first mentioned in the claims which is covered by the claims 1-4, 8, 12, 14.

Consequently, this International Preliminary Examination Report (IPER) exclusively refers to the claims 1-4, 8, 12, 14.

**Re Item V**

**Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

**1. Observations/remarks**

- 1.1 Despite the reference of claim 2 to claim 1, claim 2 is not a dependent claim in the sense of Rule 6.4(a) PCT but a concealed independent claim, because it does not include all the features of claim 1 for the following reasons:  
The feature "the second switching signal shall remain in one state throughout the period", is exchanged in favour of the feature "the second switching signal shall have a single pulse of a second determined width within the period to create a voltage pulse at the output of either +Vs or -Vs".
- 1.2 The expression "the resulting voltage at the output" implies that this feature has already been defined before, which however is not the case. For further examination it is assumed that "resulting voltage" defines a voltage pulse at the

output of the switching circuit.

1.3 In order to continue preliminary examination, the expression in claim 2, l. 22-23, "pulse widths below the minimum pulse width" is interpreted as "pulse widths of the resulting voltage at the output below the minimum pulse width".

1.4 In claims 2, 3, 4 the phrases "comprising the step of" are interpreted as "further comprising a step of" in order to introduce additional and consequently not yet defined features in the respective claim.

## 2. Prior art

Reference is made to the following documents:

D1: WO 00/74222 A (HITACHI) 7 December 2000 (2000-12-07)

D2: EP-A-0 760 552 (SGS-THOMSON) 5 March 1997 (1997-03-05)

## 3. Independent claim 1

The document D1 is regarded as being the closest prior art to the subject-matter of claim 1. Using as far as possible the wording of claim 1, document D1 discloses the following (references in the parenthesis refer to document D1):

A method of generating pulsed first and second switching signals (Fig. 15, 16: the pulsed first and second switching signals are represented by the signals PWM and DIR) for switching first and second switches (Fig. 15: transistor Q2 can be regarded as first switch; transistor Q3 can be regarded as second switch) of a switching circuit (Fig. 15) further comprising an output (Fig. 15: the output consists of the junctures Pout and Nout) and that receives a DC signal of voltage +Vs (Fig. 15: DC voltage VCC), wherein switching between various combinations of on and off states of the first and second switches (Fig. 16: curves in A and B indicate various combinations of on- and off-states of the switches, resulting from the various combinations of high H- and low L -states of the first and second switching signals DIR and PWM and lead to the voltages VCC or 0 at the junctures Pout and Nout) produces a voltage at the output with pulses at levels of +Vs, 0V and -Vs (Fig. 15, 16 A, B: The difference between the voltages of Pout and Nout can be assumed to be the "voltage at the output". With this assumption, Fig. 16 A and B immediately show that three voltage differences, and therefore three voltage levels for the voltage at the output can be obtained:  $VCC - 0 = +VCC$ ,  $VCC - VCC = 0$ ,  $0 - VCC = -VCC$ );

the method comprising the steps of:

(a) receiving a voltage demand signal indicative of a desired voltage to be supplied at

the output in a period (Fig. 16: a period can be regarded as time difference of two leading edges of the corresponding two consecutive pulses of the switching signal PWM); and

- (b) generating the first and second switching signals (Fig. 15, 16: the first and second switching signals are represented by the signals PWM and DIR) according to a first rule that the first switching signal (Fig. 15, 16: PWM signal) shall have a single pulse of a first determined width within the period (Fig. 16 A, B: As the first switching signal defines the period as time difference between two leading edges of the corresponding two consecutive pulses of the switching signal PWM, only a single pulse of the first switching signal must be within this period) and, subject to a second rule that the pulse width of the resulting voltage at the output must not fall below a minimum pulse width, that the second switching signal shall remain in one state throughout the period (in Fig. 16 A and B, the DIR signal remains constant throughout at least three periods each); the first determined width (Fig. 15: pulse width of the PWM signal) being such that the combination of the first and second switching signals when applied to the first and second switches respectively produce an average voltage at the output for the period (Fig. 15 and 16 A, B disclose that the voltage at the output between the junctures Pout and Nout can assume either the values +VCC and 0, or -VCC and 0 within a period. Consequently, each period shows an average voltage which is either between 0 and +VCC or between -VCC and 0) being substantially equal to the desired voltage.

The subject-matter of claim 1 differs from that of D1, Fig. 15 and 16 A, B, in that claim 1 additionally defines

- a control method with a voltage demand signal indicative of a desired voltage to be supplied at the output in a period with the aim to produce an average voltage at the output for the period being substantially equal to the desired voltage.
- that the pulse width of the resulting voltage at the output must not fall below a minimum pulse width.

The subject-matter of claim 1 is therefore new (Article 33(2) PCT).

D1, Fig. 4, discloses a control scheme for the current at the output of the switching circuit embodiment specified in Fig. 1 and teaches how to establish a feedback loop, a reference voltage  $V_{ref}$ , i.e. voltage demand signal, and an apparatus monitoring the output current comprising the devices RS and OP3 in order to control the current  $I_o$

between  $P_{out}$  and  $N_{out}$ , and therefore its average value. A control of the average current at the output, however, is tantamount to the control of the average voltage at the output, because the average current is proportional to the average voltage. Additionally, a voltage control seems to be already disclosed in Fig. 5. For these reasons and the fact that feedback voltage control schemes for switching circuits are standard design procedures, the person skilled in the art seems to be able to establish the average voltage control defined in claim 1 without executing an inventive step.

The problem to be solved by the present invention may therefore be regarded as how establish a control method for the switching circuit that warrants linearity of the control for all output voltages.

The solution to this problem proposed in claim 1 of the present application is considered as involving an inventive step (Article 33(3) PCT) for the following reasons:

From document D1, no hint is visible, whereupon the pulse widths of the voltage pulses at the output of the switching circuit must not fall below a minimum value. Rather, D1, abstract, teaches that the current, and consequently also the voltage across the load, can be reduced to zero by eliminating the differences in phase and pulse width duty between the input switching signals. In contrast to the definitions of claim 1, this means that there is no lower limit for the pulse width of the voltage at the output.

In D2, the embodiment of a control method for a switching circuit, represented by Fig. 2, does not allow for duty cycles of the driving signal, and therefore for the duty cycle of the output voltage, being lower than a minimum value, in order to keep up linearity of the regulation. However, this embodiment is different to that of the application, because it uses only one pulsed switching signal for driving the switching circuit instead of two pulsed switching signals, necessary for driving the switching circuit defined by the application. In a further embodiment of D2, represented by Figs. 3, 4A, 4B, which is closer to the application, because it applies two pulsed switching signals, no restrictions concerning a minimum pulse width are expressed any more, neither for the pulsed switching signals, nor for the voltage pulses at the output, while at the same time linearity of the control is warranted (cf. D2, col. 3, l. 17-23, in conjunction with col. 5, l. 25, to col. 7, l. 35).

The remaining documents cited in the International Search Report do not pick up the problem to be solved by the application at all.



#### 4. Independent claim 2

As stated under paragraph 1.1, claim 2 is an independent claim, because it does not include all the features of claim 1 it is referring to. Therefore, claim 2 can be generated by repeating claim 1 and substituting the expression "that the second switching signal shall remain in one state throughout the period" by the expression "that the second switching signal shall have a single pulse of a second determined width within the period to create a voltage pulse at the output of either +Vs or -Vs".

The document D2 is regarded as being the closest prior art to the subject-matter of claim 1. Using as far as possible the wording of claim 2, document D2 discloses the following (references in the parenthesis refer to document D2):

A method of generating pulsed first and second switching signals (abstract; Fig. 1, 3, 4A, 4B: square wave signals at control inputs C1 and C2) for switching first and second switches (Fig. 1: transistor T2 can be regarded as first switch; transistor T3 can be regarded as second switch) of a switching circuit (Fig. 1) further comprising an output (Fig. 1, 3; abstract: the output can be regarded as comprising the nodes O1 and O2) and that receives a DC signal of voltage +Vs (Fig. 1, 3: DC voltage VDD), wherein switching between various combinations of on and off states (abstract; Fig. 4A, 4B; col. 3, l. 17-23; col. 5, l. 25, to col. 7, l. 35: square waves with variable duty cycle at control inputs C1 and C2 lead to various combinations of on and off states) of the first and second switches produces a voltage at the output with pulses at levels of +Vs, 0V and -Vs (Fig. 3, 4A, 4B; col. 5, l. 25, to col. 7, l. 35: The voltage at the output can be regarded as voltage difference between the individual voltages of the nodes O1 and O2. Fig. 4A shows that the individual voltages at the nodes O1 and O2 are identical in time, which means that the voltage difference, i.e. the voltage at the output, is zero. Since the current directly corresponds to the voltage, it is zero too. Fig. 4B shows voltages at the nodes O1 and O2, which differ from each other, because the switching signal C1 has a duty cycle >50% and the second switching signal C2 has a duty cycle <50%. Consequently, the difference between these voltages, i.e. the voltage at the output, is not zero, but has voltage pulses at the output with levels +VDD or 0. Correspondingly, a duty cycle of <50% for the first switching signal C1 and a duty cycle >50% for the second switching signal C2 leads to voltage pulses at the output with levels -VDD or 0.);

the method comprising the steps of:

- (a) receiving a voltage demand signal indicative of a desired voltage to be supplied at the output in a period (Fig. 4B: For the definition of the period that square wave is significant, which has a duty cycle  $\geq 50\%$ . Taking that square wave into account,

the period can be interpreted as the time range starting at that point of time, where the leading edge of a pulse of that square wave is located and ending at that point of time, where the leading edge of the consecutive pulse of that square wave is located.); and

- (b) generating the first and second switching signals (abstract; Fig. 1, 3, 4A, 4B: square wave signals at control inputs C1 and C2) according to a first rule that the first switching signal (Fig. 1, 3: square wave signal C1) shall have a single pulse of a first determined width within the period (Fig. 4B: with the "period" as interpreted in (a) it is always warranted that only a single pulse of the first switching signal and a single pulse of the second switching signal is within the period) and, subject to a second rule that the pulse width of the resulting voltage at the output must not fall below a minimum pulse width, that the second switching signal shall have a single pulse of a second determined width within the period (Fig. 4B: with the "period" as interpreted in (a) it is always warranted that only a single pulse of the first switching signal and a single pulse of the second switching signal is within the period) to create a voltage pulse at the output of either +Vs or -Vs (Fig. 3, 4B; col. 3, l. 9-23; col. 7, l. 6-35: The voltage at the output can be regarded as the voltage difference between the individual voltages of the nodes O1 and O2. In the case of Fig. 4B, where the duty cycle of the switching signal C1 is bigger than the duty cycle of the switching signal C2, the voltage at the output has only positive pulses. Consequently, in the case, where the duty cycle of the switching signal C1 is smaller than the duty cycle of the switching signal C2, the voltage at the output has only negative pulses.); the first determined width being such that the combination of the first and second switching signals when applied to the first and second switches respectively, produce an average voltage at the output for the period being substantially equal to the desired voltage.

The subject-matter of claim 2 differs from the subject-matter of D2 in that it defines

- a voltage demand signal indicative of a desired voltage to be supplied at the output in the period instead of a desired reference current indicative of a desired current to be supplied at the output (see D2, col. 4, l. 48, to col. 5, l. 5).
- that the average voltage at the output for the period being substantially equal to the desired voltage instead of an average current at the output for the period being substantially equal to the desired average current (see D2, col. 6, l. 48, to col. 5, l. 5).
- that the pulse width of the resulting voltage at the output must not fall below a

minimum pulse width.

The subject-matter of claim 1 is therefore new (Article 33(2) PCT).

D2, col. 6, l. 4-6, in conjunction with col. 4, l. 48, to col. 5, l. 5, Fig. 3 and claim 6, discloses a control scheme regulating the average value of the current at the output O1-O2 of the switching circuit with the help of a reference voltage  $V_I$  corresponding to the desired average current.

D2 concerns the regulation of the average current with respect to a desired average current. However, it should be clear for the person skilled in the art without executing an inventive step that the average current at the output is direct proportional to the average voltage at the output. Furthermore, establishing the average voltage regulation mode instead of the average current regulation mode and vice versa, seems to be a matter of choice between a number of well known and non inventive possibilities.

The resulting problem to be solved by the present invention may therefore be regarded as how to establish a control method for the switching circuit that warrants linearity of the control for all output voltages.

The solution to this problem proposed in claim 1 of the present application is considered as involving an inventive step (Article 33(3) PCT) for the same reasons as given in paragraph 3.

#### **5. Dependent claims**

Claims 3, 4, 8, 12, 14 are dependent on the independent claims and as such also meet the requirements of the PCT with respect to novelty and inventive step.

#### **6. Industrial applicability**

The industrial applicability in the sense of Art. 33(4) PCT is given for the claims 1-4, 8, 12, 14.